

FORM PT01449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. HARL.006USF	SERIAL NO. 08/789,421
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT <i>(Use several sheets if necessary)</i>		APPLICANT Eliyahou Harari et al.	
		FILED January 29, 1997	GROUP 2785

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
LWH	A74 3 3 3 1 0 5 8	7/11/67	Perkins	340	172.5	
LWH	A75 3 4 4 2 4 0 2	5/6/69	Baxter	214	10.5	
LWH	A76 3 6 9 3 1 5 9	9/19/72	Hilberg	395	182.06	
LWH	A77 3 7 3 5 3 6 8	5/22/73	Beausoleil	365	200	
LWH	A78 3 7 5 3 2 4 4	8/14/73	Sumilas et al.	711	115	
LWH	A79 3 7 6 5 0 0 1	9/9/73	Beausoleil	365	200	
LWH	A80 3 7 7 2 6 5 2	11/13/73	Hilberg	365	200	
LWH	A81 3 7 8 1 8 2 6	12/25/73	Beausoleil	365	200	
LWH	A82 3 8 0 0 2 9 4	3/26/74	Lawlor	395	182.03	
LWH	A83 3 9 5 5 1 8 0	5/4/76	Hirtle	395	500	
LWH	A84 4 0 7 4 2 3 6	2/14/78	Ishida	365	200	

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
B25 59 - 1 5 4 5 2 5	9/1984	Japan			Abstract
B26 63 - 1 3 8 4 8 3	6/1988	Japan			Abstract
B27 63 - 1 8 4 8 8 9	7/1988	Japan			Abstract
B28 64 - 0 5 9 4 8 6	3/1989	Japan			Abstract
B29 64 - 0 7 0 8 4 3	3/1989	Japan			Abstract

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

LWH	C17	"Nonvolatility" Semiconductor vs. Magnetic," IEEE (reprint), International Solid-State Circuits Conference, February 17-19, 1998, Richard Pashley, Organizer/Moderator, p. 6-393.
LWH	C18	"High-Density Flash EEPROMS are about to Burst on the Memory Market", Electronics, March 3, 1988, J. Robert Lineback.
LWH	C19	"Erasable/Programmable solid state memories", EDN, November 14, 1985, Denny Cormier, Western Editor, pp. 145-153.

EXAMINER Ly V. Hua	DATE CONSIDERED Dec 13, 1998
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LH	A85 4 2 1 4 2 8 0	7/22/80	Halfhill et al.	360	53	
LH	A86 4 2 1 8 7 4 2	8/19/80	Carlton et al.	395	891	
LH	A87 4 2 7 7 8 2 7	7/7/81	Carlson et al.	395	500	
LH	A88 4 2 9 5 2 0 5	10/13/81	Kunstadt	711	200	
LH	A89 4 3 1 0 9 0 1	1/12/82	Harding et al.	371	10.2	
LH	A90 4 3 1 9 3 2 3	3/9/82	Ermolovich et al.	711	100	
LH	A91 4 3 9 8 2 4 8	8/9/83	Hsia et al	365	230.03	
LH	A92 4 4 2 6 6 8 8	1/17/84	Moxley	365	200	
LH	A93 4 4 4 3 8 4 5	4/17/84	Hamilton et al.	395	281	
LH	A94 4 4 6 7 4 2 1	8/21/84	White	711	118	
LH	A95 4 4 9 5 5 7 2	1/22/85	Bosen	395	500	

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B30 0 0 0 6 5 5 0	1/1980	EP	—	—	

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LH	C20	"A Reconfigurable Interconnect for In-Silicon Electronic Assembly", 32nd Electronic Components Conference, May 10-12, 1982, Hsia et al., pp. 7-16.
LH	C21	"Adaptive Wafer Scale Integration", Japanese Journal of Applied Physics, vol. 19, supp. 19-1, 1980, Yukun Hsia et al., pp. 193-202.
LH	C22	"Nonvolatile Memories: A 5V-Only 256k Bit CMOS Flash EEPROM", 1989 IEEE International Solid State Circuits Conference, No. 0193-6530/89/0000-0132, February 16, 1989, D'Arrigo et al, pp. 132-133.

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<i>RWH</i>	A96	4	5	0	6	3	2	4		3/19/85	Healy	395	500	
<i>RWH</i>	A97	4	5	0	9	1	1	3		4/2/85	Heath	395	886	
<i>RWH</i>	A98	4	5	7	3	1	4	1		2/25/86	Simon	395	500	
<i>RWH</i>	A99	4	5	7	8	7	7	4		3/25/86	Muller	395	750.06	
<i>RWH</i>	AA1	4	5	8	4	6	8	1		4/22/86	Singh et al	395	182.05	
<i>RWH</i>	AA2	4	6	3	0	2	3	0		12/16/86	Sundet	711	169	
<i>RWH</i>	AA3	4	6	3	8	4	6	5		1/20/87	Rosini et al.	365	228	
<i>RWH</i>	AA4	4	6	4	4	4	9	4		2/17/87	Muller	711	152	
<i>RWH</i>	AA5	4	6	4	8	0	7	6		3/3/87	Schrenk	365	189.01	
<i>RWH</i>	AA6	4	6	5	4	8	2	9		3/31/87	Jiang et al.	365	189.03	
<i>RWH</i>	AA7	4	6	8	0	7	3	6		7/14/87	Schrenk	365	218	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>RWH</i>	C23	"Nonvolatile Memories: An Experimental 4Mb CMOS EEPROM with a NAND Structured Cell", IEEE International Solid State Circuits Conference, No. 0193-6530/89/0000-0134, February 16, 1989, Itoh et al., pp. 134-135.
<i>RWH</i>	C24	"Nonvolatile Memories: A 90ns 100k Erase/Program Cycle Megabit Flash Memory", IEEE International Solid State Circuits Conference, No. 0193-6530/89/0000-0140, February 16, 1989, Kynett et al., pp. 140-141.
<i>RWH</i>	C25	"An In-System Reprogrammable 32K x 8 CMOS Flash Memory", IEEE Journal of Solid State Circuits, vol. 23, no. 5, October 1988, Kynett et al., pp. 1157-1161.

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LWH	AA8 4 6 8 8 1 7 0	8/18/87	Waite et al.	395	500	
LWH	AA9 4 7 1 3 7 5 6	12/15/87	Mackiewicz et al.	365	228	
LWH	AB1 4 7 3 3 3 7 5	3/22/88	Terashima	365	185.23	
LWH	AB2 4 7 3 7 9 3 5	4/12/88	Wawersig et al.	365	200	
LWH	AB3 4 7 4 4 0 6 2	5/10/88	Nakamura et al.	365	185.04	
LWH	AB4 4 7 4 8 3 2 0	5/31/88	Yorimoto et al.	235	492	
LWH	AB5 4 7 5 0 1 5 8	6/7/88	Giebel et al.	365	200	
LWH	AB6 4 7 5 1 7 0 3	6/14/88	Picon et al.	395	182.06	
LWH	AB7 4 7 8 0 8 5 5	10/25/88	Iida et al.	365	185.22	
LWH	AB8 4 7 8 3 7 4 5	11/8/88	Brookner et al.	705	410	
LWH	AB9 4 7 8 9 9 6 7	12/6/88	Liou et al.	365	218	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

LWH	C26	"Nonvolatile Memories: A 1Mb Flash EEPROM", IEEE International Solid State Circuits Conference, No. 0193-6530/89/0000-0140, February 16, 1989, Cernea et al.
LWH	C27	"Semidisk Disk Emulator", Interface Age, pp. 102, November 1982.

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<i>RW</i>	AC1	4	7	9	1	6	0	4		12/13/88	Lienau et al.	365	9	
<i>RW</i>	AC2	4	7	9	1	6	1	5		12/13/88	Pelley III et al.	371	10.3	
<i>RW</i>	AC3	4	8	0	3	5	5	4		2/7/89	Pape	348	231	
<i>RW</i>	AC4	4	8	1	7	0	0	2		3/28/89	Sansone et al.	705	405	
<i>RW</i>	AC5	4	8	5	3	8	5	3		8/1/89	Yamamura et al.	705	20	
<i>RW</i>	AC6	4	9	3	1	9	4	3		6/5/90	Vermesse	705	404	
<i>RW</i>	AC7	4	9	3	9	5	9	8		7/3/90	Kulakowski et al.	360	48	
<i>RW</i>	AC8	4	9	6	4	0	7	4		10/16/90	Suzuki et al.	395	500	
<i>RW</i>	AC9	4	9	7	7	5	0	3		12/11/90	Rudnick et al.	364	40.1	
<i>RW</i>	AD1	4	9	8	4	1	9	1		1/8/91	Vermesse	705	410	
<i>RW</i>	AD2	5	1	4	6	5	7	1		9/8/92	Logan	395	182.06	

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LW	AD3	5 1 6 7 0 2 1	11/24/92	Needham	395	836	
LW	AD4	5 2 1 8 6 9 1	6/8/93	Tuma et al.	395	500	
LW	AD5	5 2 2 6 1 3 6	7/6/93	Nakagawa	463	44	
LW	AD6	5 2 3 9 6 6 2	8/24/93	Danielson et al.	395	200.78	
LW	AD6	5 2 5 3 3 5 0	10/12/93	Foster et al.	711	202	
LW	AD7	4 8 8 2 4 7 4	11/21/89	Anderi et al.	235	380	

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